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NO. 243 P. 1

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# FACSIMILE COVER SHEET

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:  
KUMAR ET AL.

Serial No. 10/611,322

Confirmation No. 4030

Filing Date: JULY 1, 2003

For: DIGITAL ELECTRONIC CIRCUIT  
FOR TRANSLATING HIGH VOLTAGE  
LEVELS TO LOW VOLTAGE LEVELS

Attorney Docket No.  
52669\_CIP1

REQUEST FOR CORRECTION TO THE FILING RECEIPT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The filing receipt for the subject patent application has been received and reviewed for accuracy. Three discrepancies have been discovered. The filing receipt in error lists the address of the second inventor as "Pithoragarh, India". The correct address of the second inventor is Uttaranchal, India. The next error lists the address of the Assignee as "Noida, India". The correct address of the Assignee is Uttar Pradesh, India. Lastly the filing date for foreign application no. 706/DEL/2002 is listed as "07/01/03". The correct filing date for foreign application no. 706/DEL/2002 is 07/01/02.

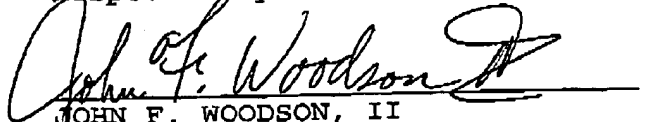
In view of the errors noted, it is respectfully requested that a corrected filing receipt be issued in this

In re Patent Application of:  
KUMAR ET AL.  
Serial No. 10/611,322  
Filing Date: JULY 1, 2003

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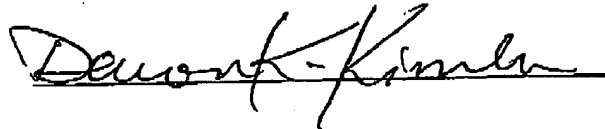
application. If any fee is believed to be necessary,  
authorization is given to charge Deposit Account No. 01-0484.

Respectfully submitted,

  
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Attorney for Applicants

CERTIFICATE OF FACSIMILE

I HEREBY CERTIFY that this REQUEST FOR CORRECTION TO  
THE FILING RECEIPT for U.S. Serial No. 10/611,322 is being  
submitted via telefacsimile no. 703-746-9195 to: OFFICE OF  
INITIAL PATENT EXAMINATION'S FILING RECEIPT CORRECTIONS, P.O.  
BOX 1450 ALEXANDRIA, VA 22313-1450, this 23rd day of January,  
2004.



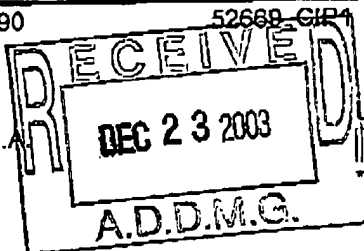


## UNITED STATES PATENT AND TRADEMARK OFFICE

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/611,322	07/01/2003	2816	990	52689-CIP4	14	25	3

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CONFIRMATION NO. 4030

UPDATED FILING RECEIPT



\*0C00000011537649\*

Date Mailed: 12/19/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

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Sunil Chandra Kasanyal, ~~Pithoragarh~~, INDIA;  
*Uttaranchal*

## Assignment For Published Patent Application

STMicroelectronics Pvt. Ltd., Noida, INDIA;  
*Uttar Pradesh*

## Domestic Priority data as claimed by applicant

This application is a CIP of 10/460,044 06/12/2003

## Foreign Applications

INDIA 635/DEL/2002 06/13/2002  
INDIA 706/DEL/2002 ~~07/01/2003~~  
*7/01/02*

If Required, Foreign Filing License Granted: 09/25/2003

Projected Publication Date: 04/01/2004

Non-Publication Request: No

Early Publication Request: No

**Title**

Digital electronic circuit for translating high voltage levels to low voltage levels

**Preliminary Class**

327

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Title 37, Code of Federal Regulations, 5.11 & 5.15**

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